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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		Application Number	10/821,505
		Filing Date	April 9, 2004
		First Named Inventor	Steve C. Huang
		Art Unit	3612
		Examiner Name	LIN, SUN J.
Sheet one of one	Attorney Docket Number	ID-04-01	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
JSR		DEREK L BEATTY et al., Formally Verifying A Microprocessor Using a Simulation Methodology, 1994, 31st ACM/IEEE Design Automation Conference, pp. 596-602	
		ALFRED KOLBL et al., Symbolic RTL Simulation, 2001, DAC 2001, pp.47-52	
		SRIRAM C. KRISHNAN et al., Symbolic Simulation Formally Verifies ECC, April 2, 2002, EEdesign.	
		ACCULOGIC Web page, Boundary Scan, 2003.	
		JTAG Technologies Web page, Unlocking the power of Boundary-scan, 2001.	
JSR		MARCUS HEDLUND, The Standard for Embedded Core Test, 7 pages, University of Jonkoping, School of Engineering, Sweden	

Examiner Signature	<i>James Sun</i>	Date Considered	1-17-06
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\*EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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